

Application No.: 10/720,759
Request for Reconsideration
Reply to Office Action dated September 23, 2005
January 19, 2006

REMARKS

Currently, claims 1-20 are pending in the application.

Independent claims 1 and 16 along with dependent claims 4, 6, 8, 10-13, 18 and 20 were rejected under 35 USC 103(a) as being obvious over the Admitted prior art in view of Japanese Patent Publication No. 3-145178 (hereinafter JP03145178).

Dependent claims 2-3, 5, 7, 14 and 17 were also rejected under 35 USC 103(a) as being obvious over the Admitted prior art in view of JP03145178 and further in view of Hsu (U.S. Patent Application Publication No. 2004-0108804).

Further, dependent claims 9 and 19 were rejected under 35 USC 103(a) as being obvious over the Admitted prior art in view of JP03145178 and further in view of Ko et al. (U.S. Patent No. 5,436,466).

Finally, independent claim 15 was rejected under 35 USC 103(a) as being obvious over the Admitted prior art in view of JP03145178 and further in view of Hsu.

All of these rejections are based on the combination of the Admitted prior art shown in Figs. 5 and 6 of the present application in view of JP03145178.

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These rejections are respectfully traversed in view of the following remarks.

Claims 1, 15 and 16 are the independent claims in the application and they all recite an intermediate layer as discussed below.

Independent claim 1 recites "an intermediate layer is disposed between said p-side ohmic electrode and said p-side pad electrode so as to cover a portion of said p-side ohmic electrode including an area that covers said top face of said ridge".

Independent claim 15 recites the phrase of claim 1 above and also recites "wherein said intermediate layer includes a diffusion prevention means for preventing diffusion of a low melting point".

Independent claim 16 also recites "an intermediate layer is disposed between said p-side ohmic electrode and said p-side pad electrode so as to cover a portion of said p-side ohmic electrode including an area that covers the top face of said ridge and said intermediate layer is an insulator".

In the office action, the Examiner stated that the Admitted prior art does not show an intermediate layer. Applicant respectfully submits that the Examiner must also be of the opinion that that the Admitted prior art does not show an intermediate

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layer disposed between a p-side ohmic electrode and a p-side pad electrode so as to cover a portion of the p-side ohmic electrode including an area that covers a top face of the ridge as claimed in independent claims 1, 15 and 16.

The Examiner believed that JP03145178 taught in Fig. 1d, a single intermediate layer (insulator) 4 disposed between the electrodes 2 and 5. The Examiner also believed that it would have been obvious to provide the Admitted prior art with what is taught by JP03145178 for the reason of electrically insulating the electrodes from each other.

Applicant respectfully submits that the combination of the Admitted prior art and JP03145178 is not proper.

Further, Hsu does not make up for the deficiencies in the Admitted prior art and JP03145178. Hsu relates to a field emitter cell including a thin-film-edge emitter normal to the gate layer. Hsu discloses that the thin-film-edge emitter may also be included into nanofilaments. However, the intermediate layer (buffer layer) in Hsu is disposed between an inner conductive layer and a catalyst layer. This is completely different from an intermediate layer disposed between a p-side ohmic electrode and a p-side pad electrode so as to cover a

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portion of the p-side ohmic electrode including an area that covers the top face of the ridge as recited in claims 1, 15 and 16.

Further, applicant respectfully submits that there is no teaching or suggestion in the Admitted prior art, JP03145178 and Hsu, to suggest combining these references in a manner to make the present claims obvious.

Ko et al. do not make up for the deficiencies in the Admitted prior art, JP03145178 and Hsu. Ko et al. disclose an intermediate layer having at least two layers but these are disposed in the semiconductor layer. This is completely different from an intermediate layer disposed between a p-side ohmic electrode and a p-side pad electrode so as to cover a portion of the p-side ohmic electrode including an area that covers the top face of the ridge as recited in claims 1, 15 and 16.

In view of foregoing claim amendments and remarks, it is respectfully submitted that the application is now in condition for allowance and an action to this effect is respectfully requested.

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If there are any questions or concerns regarding the amendments or these remarks, the Examiner is requested to telephone the undersigned at the telephone number listed below.

Respectfully submitted,

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Randolph A. Smith
Reg. No. 32,548

SMITH PATENT OFFICE
1901 Pennsylvania Ave., N.W.,
Suite 901
Washington, DC 20006-3433
Telephone: 202/530-5900
Facsimile: 202/530-5902
Matsumura011906